Overview of one transistor type of hybrid organic ferroelectric non-volatile memory

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Abstract: Organic ferroelectric memory devices based on field effect transistors that can be configured between two stable states of on and off have been widely researched as the next generation data storage media in recent years. This emerging type of memory devices can lead to a new instrument system as a potential alternative to previous non-volatile memory building blocks in future processing units because of their numerous merits such as cost-effective process, simple structure and freedom in substrate choices. This bi-stable non-volatile memory device of information storage has been investigated using several organic or inorganic semiconductors with organic ferroelectric polymer materials. Recent progresses in this ferroelectric memory field, hybrid system have attracted a lot of attention due to their excellent device performance in comparison with that of all organic systems. In this paper, a general review of this type of ferroelectric non-volatile memory is provided, which include the device structure, organic ferroelectric materials, electrical characteristics and working principles. We also present some snapshots of our previous study on hybrid ferroelectric memories including our recent work based on zinc oxide nanowire channels.

Key words: organic ferroelectric; field effect transistor; non-volatile; memory; hybrid

1 Introduction

Ferroelectric random-access memory (FeRAM) was conceptualized in 1952 by an MIT postgraduate student, Dudley Allen Buck, while undertaking his master's thesis [1]. In 1995, a NASA researcher developed a novel method for fabricating nondestructive readout devices [2]. FeRAM has continued to attract intense interest as a replacement of traditional flash memory materials to improve the performance. Organic ferroelectrics offer additional advantages such as good remnant polarization, fast switching time, and ease of film formation in ambient environments [3-5]. FeRAM maintains the programmed data after main-power cutoff as a flash memory but is much faster than a flash memory [6]. Consequently, FeRAM is expected to replace current commercial memory devices and become the mainstay of future wireless instrument applications. Ferroelectric field effect transistor (FeFET) memory devices are more simply structured than FeRAM devices, because their dielectric layer is replaced by ferroelectric materials without the extra memory capacitance of FeRAM. Therefore, FeFET devices can be fabricated at low cost and on smaller scales than is possible in the normal silicon industry roadmap [7]. As information technology (IT) expands and diversifies and technologies such as internet of things (IoT) emerge, a data-driven world is expected in the near future. Data control innovations and storage devices such as FeFETs should concomitantly adapt to this new era [8]. A FeFET device comprising one field effect transistor (FET) with ferroelectric materials in its gate insulator layer is called a one-transistor (1T)-type FeFET. Moreover, on account of their flexibility, organic ferroelectric materials are being considered as an alternative nonvolatile memory. All organic structures can feasibly realize flexible devices; therefore, previous studies have focused on organic semiconductor channel materials [9-16]. However, because of their low mobility, high operating voltage and very weak ambient air stability, organic semiconductors cannot rival inorganic semiconduc-

tors in memory applications demanding high-speed data processing. Recently, some groups have been developing hybrid FeFETs, composites of organic ferroelectrics and inorganic semiconductors. Hybrid FeFETs exhibit several desired properties of a high performance device such as good data retention time characteristics, endurance, program speed and flexibility [17-24]. In this review, we will cover various applications of hybrid 1T-type organic ferroelectric memory devices. We then introduce emerging applications of organic ferroelectrics based on functional nanomaterials, namely, zinc oxide nanowires grown by chemical vapor deposition, which were recently investigated by our group. We also briefly discuss novel device concepts, and the structures and operating principles of organic ferroelectric materials.

2 Organic ferroelectric

An FET-based nonvolatile memory (NVM) substitutes the standard dielectric layer with a ferroelectric layer in the device structure. Various organic polymers exhibit a memory-like response to an external energy source [5, 16, 25, 26]. Among these, poly (vinylidenefluoride-co-trifluoroethylene) (P(VDF-TrFE)) has been extensively researched because its characteristics are deemed suitable for NVM. This paper considers P(VDF-TrFE) as primarily responsible for the functionality of ferroelectric copolymers. Ferroelectric materials undergo spontaneous polarization (Ps), thus present a remnant polarization (Pr) in the absence of an external electric field. The Ps is reversed when the externally applied voltage exceeds the coercive field (E_c). Consequently, ferroelectric materials exhibit nonlinear properties that depend on the frequency and intensity of the external electric field [27]. Fig. 1 shows the reversal of spontaneous polarization in the hysteresis loop. Ps arises from the movement of dipoles in the crystalline structure, which is induced by ferroelectricity and is aligned by the electric field [28]. The dipole polarization can be reversed by reversing the electric field [29]. Fig. 2 displays the molecular structure and ferroelectric switching of P(VDF-TrFE) [30]. The different electron affinities of fluorine and hydrogen atoms in ferroelectric materials establish a dipole moment between the two atom types [31]. To estimate the characteristics of P(VDF-TrFE), we must determine the hysteresis loop and obtain the capacitance-voltage (C-V) measurements. These measurements yield important information such as the Ps and Pr, coercive field, and coercive voltage (V_c). Fig. 3 presents a Sawyer-Tower circuit system, used to obtain the ferroelectric capacitor characteristics. Introduced in 1930 [32], this classic circuit remains useful for measuring ferroelectric properties. In Fig. 3, the oscilloscope steering plates of the original circuit are replaced by reference capacitors and the output signal is directed into the high-impedance input of an oscilloscope.

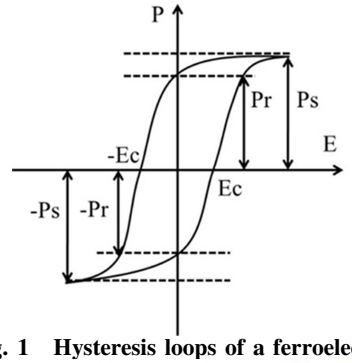

Fig. 1 Hysteresis loops of a ferroelectric

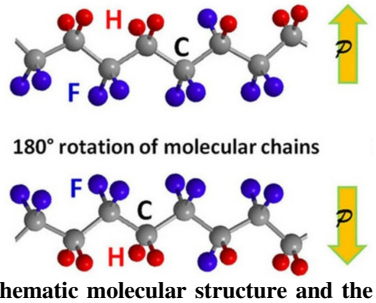

Fig. 2 Schematic molecular structure and the switching of the P(VDF-TrFE) [30] Copyright 2014, Nature

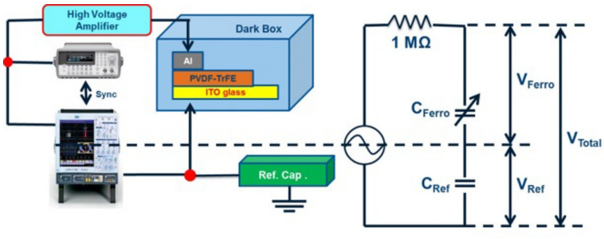

Fig. 3 Schematic of a Sawyer-Tower circuit and equivalent circuit.

The two-capacitor Sawyer-Tower circuit comprises the reference capacitor and a ferroelectric sample in series with the reference capacitor. The polarization is calculated as follows:

$$P = Q/A \quad (1)$$

$$Q = C \times V \quad (2)$$

where Q is the charge, A is the area of the top electrode, C is the reference capacitance, and V is the measured voltage. To ensure that most of the applied voltage shunts across the ferroelectric capacitor, the reference capacitance should be much larger than the capacitance of the ferroelectric material. The vertical and horizontal axes of the oscilloscope represent the applied voltage and the polarization of the ferroelectric sample, respectively. The hysteresis loops of a P(VDF-TrFE) ferroelectric copolymer with thicknesses of 150, 200, and 250 nm are displayed in Figs. 4, 5, and 6, respectively. The hysteresis loops in Fig. 4 are distorted, indicating significant current leakage in the thin copolymer layers; moreover, the spontaneous polarization produces an insufficient electric field. The 200 nm thick polymers yielded a properly shaped hysteresis loop but required a high electric field to reach the target Pr due to the leakage current between the bottom ITO electrode and the top Al electrode. Therefore, the hysteretic behaviors depend on the thickness of copolymers annealed at the same temperature. In this case, the annealing temperature (140℃) was near the Curie temperature (Tc), which is important for Ps. Thin copolymers annealed above or below the Curie temperature can alter their structures, thereby behave similarly to nonpolar dielectrics. The ferroelectric characteristics are easily and popularly determined by constructing a C-V curve. Because the domain structure of the ferroelectric material leads to nonlinear polarization, the C-V characteristics exhibit a butterfly shape, depending on whether the applied electric field is positive or negative. The C-V plot peaks at the coercive voltage V_c. As shown in Figs. 7, 8, and 9, the C-V characteristics depend on the annealing temperature and frequency. At low and high an

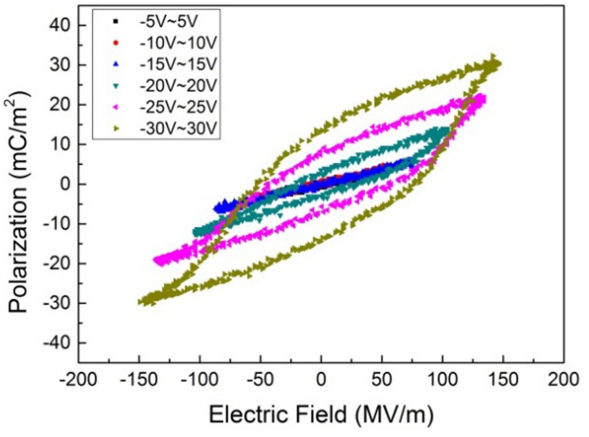

Fig. 4 Hysteresis loop of the 5wt% P(VDF-TrFE) thickness of 150 nm at 140 ℃

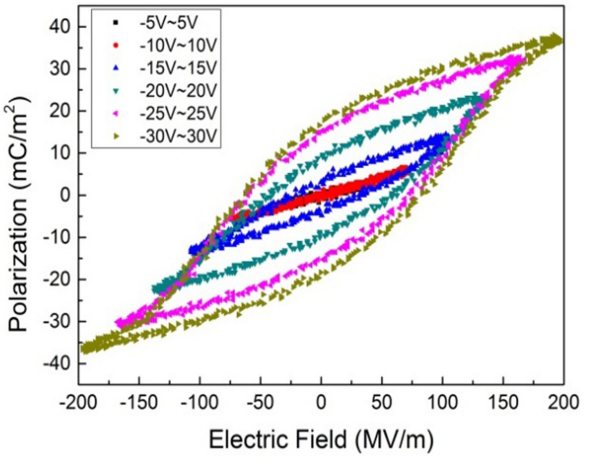

Fig. 5 Hysteresis loop of the 5wt% P(VDF-TrFE) thickness of 200 nm at 140 ℃

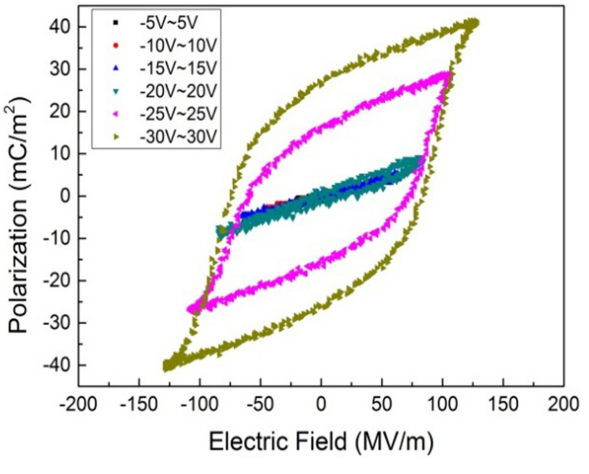

Fig. 6 Hysteresis loop of the 5wt% P(VDF-TrFE) thickness of 250 nm at 140 ℃

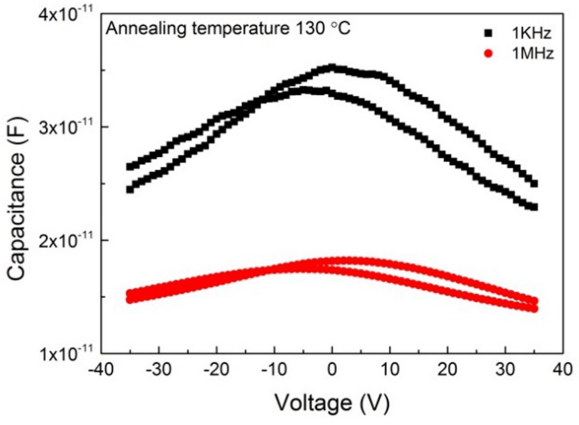

Fig. 7 C-V characteristic of the P(VDF-TrFE) at annealing temperature of 130 ℃

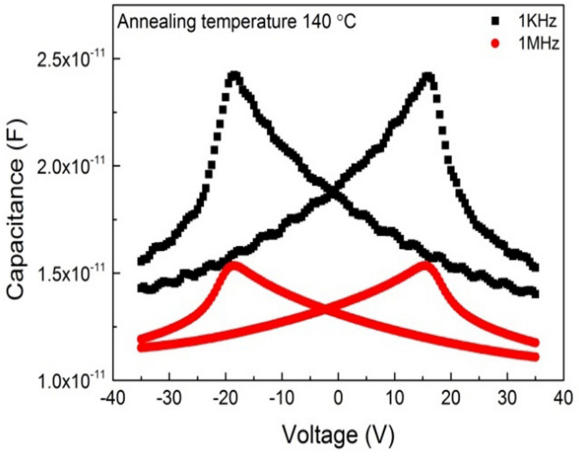

Fig. 8 C-V characteristic of the P(VDF-TrFE) at annealing temperature of 140 ℃

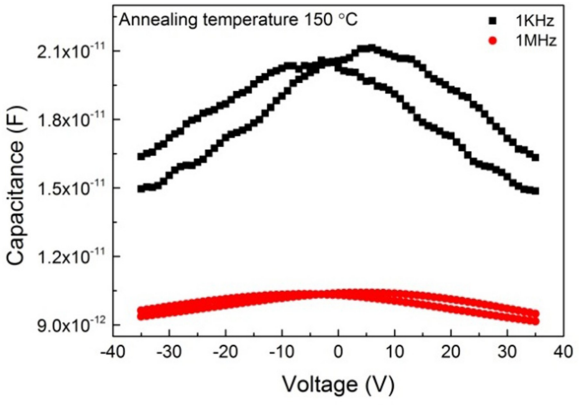

Fig. 9 Characteristic of the P(VDF-TrFE) at annealing temperature of 150 ℃

nealing temperatures, the C-V properties show no significant peaks at high applied voltages. However, at the optimal annealing temperature, peaks of equal height appear and the butterfly-shaped curve is clearly defined. Annealing is the crucial step, as it forms the crystallites of P(VDF-TrFE) that determine the ferroelectric characteristics. Here the important parameter is the annealing temperature. Copolymer crystallinity normally forms between the Curie temperature and the melting temperature [33].

3 Hybrid 1T FeFET

Organic nonvolatile FeFET memory devices can be classified into two types: all-organic devices and organic ferroelectric mixed with an inorganic semiconductor layer. The second class that includes hybrid FeFETs displays excellent device performance and stability in ambient air. Conversely, all-organic devices are robust to flexibility, but their very high voltage for data programming and low operating speed renders them unsuitable for modern instruments and signal process units. For these reasons, hybrid structures have begun emerging as viable alternatives.

3.1 Working principle of FeFET

Fig. 10 shows the basic structures of the capacitor and FeFET models [34]. The mechanism is complicated in organic materials because the amorphous structure cannot be explained authentically. The intrinsic memory phenomenon of FeFETs results from the behavior of the carrier state in the semiconductor channel. The possible conductance states are on and off (see Fig. 11). When a (positive or negative) gate voltage is applied to the gate electrode, the ferroelectric polarization realigns in the direction of the interface between the ferroelectric and semiconductor layers. Moreover, the on/off state of the FeFET device is driven by the depletion or accumulation of electrons[34].

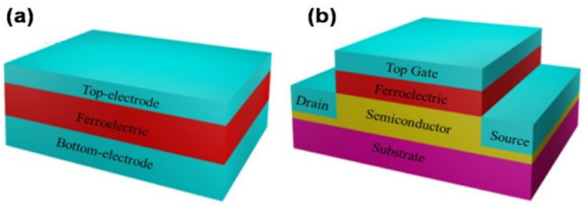

Fig. 10 (a) The capacitor model, consisting of a thin ferroelectric film between two conductive electrodes. (b) The FeFET model, which replaces the dielectric of MOSFET with ferroelectric [34]. Copyright 2012, Springer.

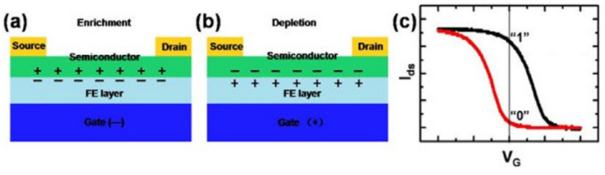

Fig. 11 Schematic views of p-type FeFET and corresponding hysteretic loop of polarization. (a,b) Schematic views of p-type FeFET for a simplified field-effect transistor model. (c) The corresponding hysteretic loop of polarization varies with the external electric field [34].

3.2 FeFET channel layer

The performance factors of the semiconductor channel layer such as operating voltage, on/off ratio, retention time, endurance cycle number, and flexibility depend on the layer composition. The most common semiconductors in hybrid FeFETs are traditional thin-film semiconductors such as zinc oxide (ZnO). Fig 12 is a schematic of a FeFET device with a channel layer of indium-gallium-zinc oxide (IGZO). The performance of the device is presented in Fig. 13. The device shows an excellent on/off ratio and a low operating voltage (10^9 and 15 V, respectively) [18]. Figs. 14 and 15 display a schematic cross-section of a hybrid type & organic semiconductor FeFET and the characteristics of P(VDF-TrFE), respectively. The operating voltage, memory window, and retention time of this hybrid type device are 20 V, 20 V, and 10000 s, respectively [20]. Overall, organic semiconductor-based FeFETs operate over 40-150 V with an on/off ratio of 104 and endure for 100 cycles [10, 15, 35, 36]. Note that the hybrid FeFET is technically superior to any organic FeFET. Thin-film type FeFET semiconductors also suffer from various problems. In general, the coercive field (E_C) of the thin film is several kilovolts per centimeter. Consequently, the FeFET requires a high operating voltage to repolarize the ferroelectric. Such high voltage can disorder the organic materials. Furthermore, unless the organic ferroelectric is carefully purified, the numerous holes and defects provoke a large gate leakage current, which decreases the memory window and adversely affects the retention time characteristics of the FeFET device. In recent years, nanowire semiconductors have been considered as promising building blocks of FeFET semiconductor layers, on account of their nanoscale dimensions and high performance traits for active channel layers. Nanowires are particularly promising candidates for mechanically robust devices and have been incorporated in diverse applications. Inorganic semiconducting nanowires (NWs), which exhibit high performance and air stability, are the envisaged building blocks of future functional nanoscale devices. Among these, ZnO NWs are among the leading candidates for electronics and optoelectronics as they can be synthesized with high crystallinity at low cost. Furthermore, because of their high field-effect mobility and excellent conductance modulation properties, ZnO NWs are suitable transistor channel materials in FeFET based memory applications [22]. Fig. 16 is a three-dimensional schematic of the final FeFET device structure fabricated with ZnO NWs. Unlike P(VDF-TrFE)-based ZnO thin film memory devices [37], the new structure requires no dielectric layer (as a buffer gate) or photolithographic gate patterning to reduce the gate leakage current. Fig. 17 shows the electrical transfer characteristics (I_{DS}-V_{GS}) and the gate leakage current of the FeFET measured under V_{DS} = 0.1V while the V_G was ranged from −20V to +20V at 0.2 V/s. For comparison, the inset shows the $I_{DS}-V_{GS}$ curve of a typical ZnO NW FET.

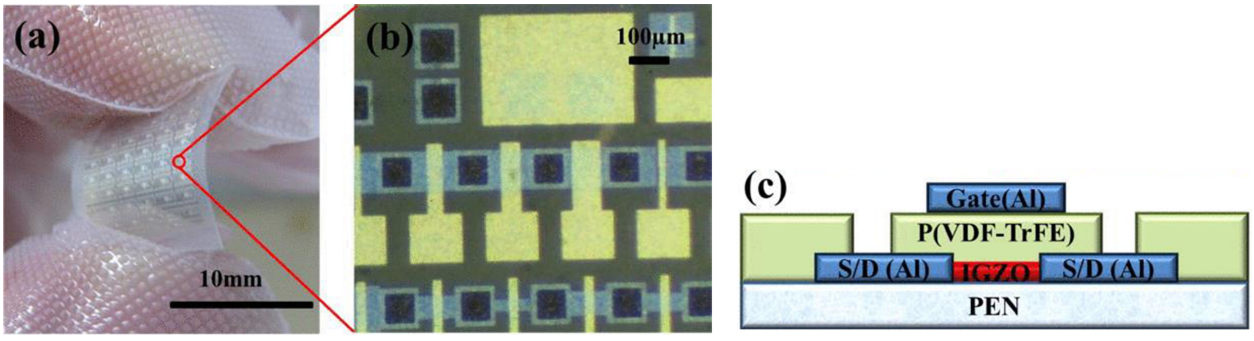

Fig. 12 (a) The photograph and (b) photomicrograph of the fabricated Fe-TFTs, respectively. (c) Cross-sectional schematic diagram with Al/P(VDF-TrFE)/IGZO/Al/PEN structure [18]. Coryright 2011 American Institute of Physics

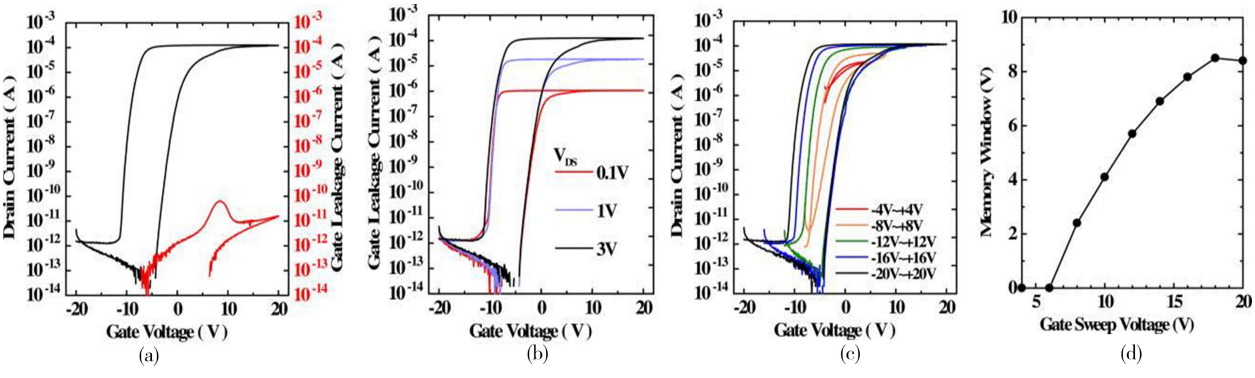

Fig. 13 Sets of I_D-V_G transfer curve of (a) I_D-V_G transfer curve and gate leakage current, (b) I_D-V_G transfer curves according to the drain voltage (V_D=0.1, 1, 3 V), (c) I_D-V_G transfer curve with the range of the gate sweep voltage, and (d) the change of the memory window (MW) according to the gate sweep voltage for the fabricated Fe-TFTs [18]. Coryright 2011 American Institute of Physics

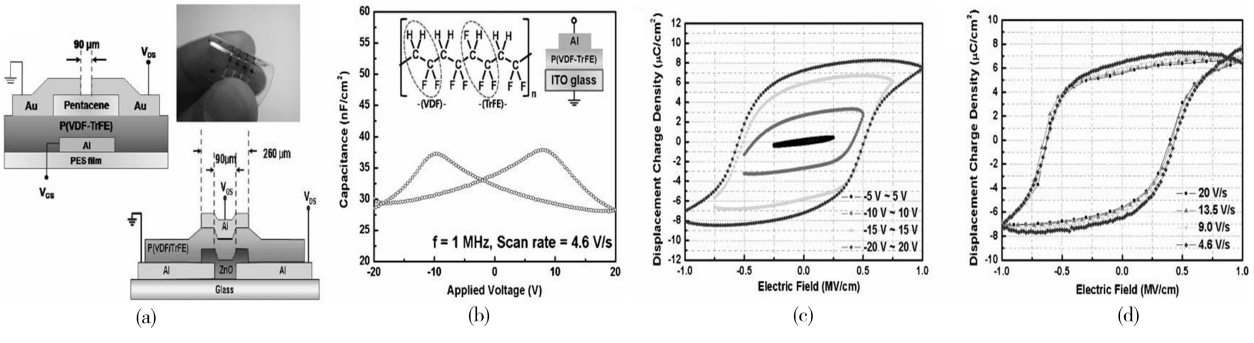

Fig. 14 (a) Schematic cross-section of our bottom-gate pentacene and top-gate ZnO NVM-TFTs with P(VDF-TrFE) ferroelectric polymer layers. The photograph of a flexibl pentacene NVM-TFT on a PES films is also presented. b) Capacitance-voltage (C-V) curves of the 200-nm-thick P(VDF-TrFE) as obtained by quenching after curing at 160 ℃ on ITO glass (1 MHz, scan rate of 4.6 V s^{-1}). c) Pr-E curves of the 200-nm-thick P(VDF-TrFE) as a function of gate voltage (scan rate of 4.6 V s^{-1}). d) Pr-E curves as a function of scan rate (4.6-20 V s^{-1}) [20]. Copyright 2011 John Wiley & Sons.

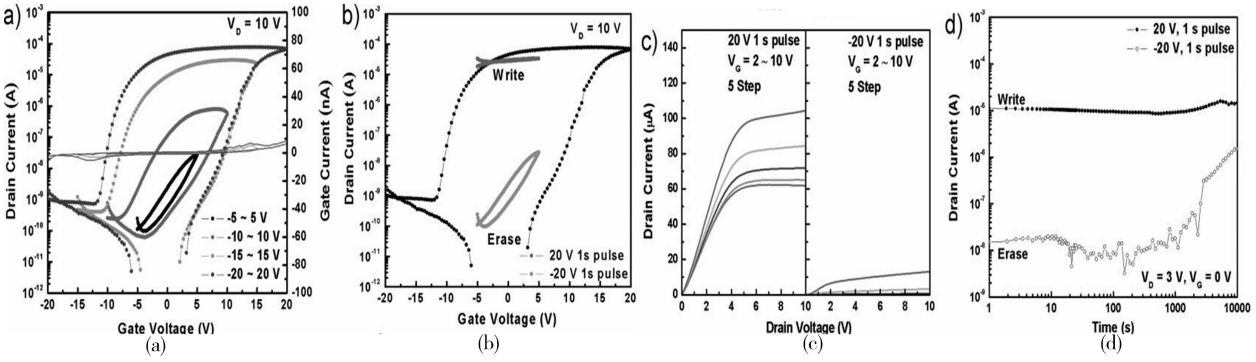

Fig. 15 (a) Transfer curves and memory hysteresis of top-gate ZnO NVM-TFTs as a function of gate voltage, obtained in several V_G ranges under V_D = 10 V. b) Transfer curves obtained in ±5V V_G range after pulses for write (-20 V, 1 s) and erase (-20 V, 1 s). The curves were compared with the full range (-20 V to 20 V) transfer curves. c) I_D-V_D output curves of write and erase states. d) Retention properties of write and erase states recorded under V_D = 3V, V_G = 0 V, for 10000 s [20]. Copyright 2011 John Wiley & Sons.

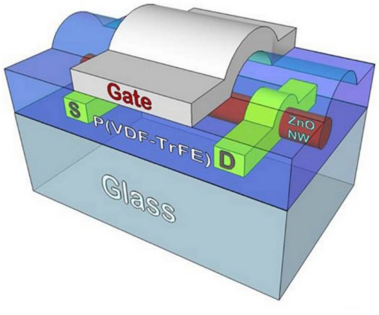

Fig. 16 A 3D schematic representation of the ferroelectric non-volatile memory device based on a top-gateZnO NW FET with a ferroelectric copolymer gate insulator[22]

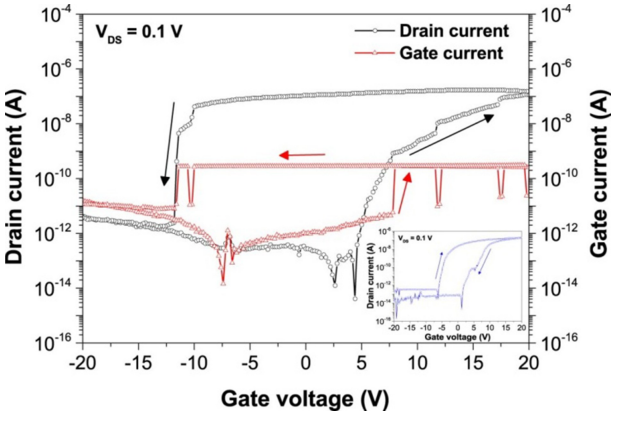

Fig. 17 Electrical transfer characteristics (I_{DS}-V_{GS}) and the gate leakage current (y-axis on the right) of the FeFET memory device measured under V_{DS} = 0.1V at a scan rate of 0.2V/s and a scan range from −20V to +20V. The inset shows the I_{DS}-V_{GS} curve [22].

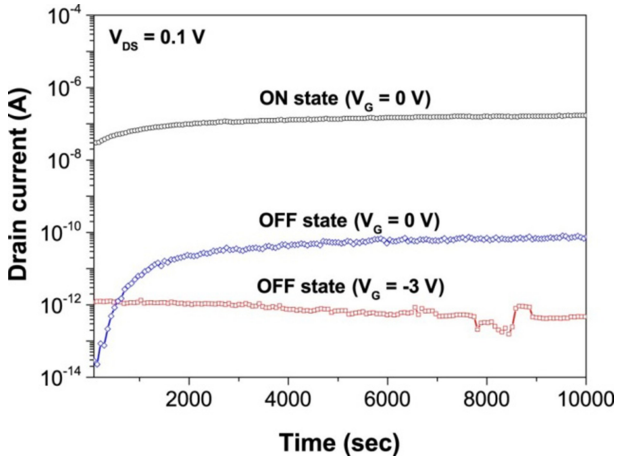

Fig. 18 Data retention characteristics of the memory device's ON and OFF states after application of a writing pulse (+25V, 2s) and an erasing pulse (−25V, 2s), respectively. The time evolution of the drain current was evaluated under V_{DS} = 0.1V for over 10^4 s with two different V_G values examined for the OFF state (V_G = 0 V and V_G = -3 V) [22].

The estimated coercive voltage in the 200-nm-thick P(VDF-TrFE) layer (~20 V) is in excellent agreement with our selected I_{DS}-V_{GS} scan range. The device displays a high on-current (>0.1μA) at V_G =20V, and an excellent remnant current modulation (> 10^5) at V_G = 0V. A counterclockwise memory hysteresis window of 16.5V is observed, and the

gate leakage current is below 300pA. The hysteresis direction indicates the switching behavior of the electric dipoles in the ferroelectric polymer layer [22]. Fig. 18 demonstrates the data retention properties of the memory device in the ON and OFF states, evaluated over 10^4 s. During the evaluation we set V_{DS} = 0.1V, and we set V_G in the OFF state as V_G = 0V or V_G = −3V [22]. The gate terminal was given an initial pulse of V_G = ±25V for 2 s, and the evolution of the drain current was recorded. The V_G pulse aligns the electric dipole moments in the P(VDF-TrFE) layer in the direction of the gate electric field. If the pulse is positive (negative), electrons are accumulated (depleted) at the surface of the n-type ZnO NW and conductance modulation occurs [22]. When the initial pulse was followed by a continuous V_G of −3 V, the ON state current in steady-state slightly increased while the OFF state current remained relatively stable at 10^{-12} A. However, after applying V_G = 0V for 10^4 s, the OFF state current degraded by two decades[22]. This effect would occur if an intrinsic channel-induced depolarization field remained after removing the gate bias. Such a field would reduce the retention time in the OFF state[22].

4 Conclusions

Organic ferroelectric memory materials have attracted considerable attention due to their advantages such as non-volatile nature, low cost, easy fabrication, and flexibility. However, there are still substantial challenges for real applications. The FeFET devices demonstrated so far can be further improved significantly by using hybrid structures to achieve low operating voltages, long retention time, high endurance cycles and robustness in ambient air. If the remaining scientific issues are solved, the FeFET will facilitate the development of next generation memory process unit of instrument applications.

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